

Airborne Telemetry

NBM-A429-8 NetDAS

Airborne Data Acquisition Products

FEATURES

- Each input port meets the characteristics described in the Mark 33 Digital Information Transfer System (DITS) ARINC-429 Specification 429-12 published July 1, 1990.
- Each input can be independently programmed for low speed (12.0-14.5 kbps) or for high speed (100.0 kbs) operation.
- Each label can be independently programmed for 8 bit addressing (label only) or for 10 bit addressing (label and SDI).
- Programmable to acquire 377 octal labels from each bus.
- Programmable to concurrently acquire 4 source/data identifier (SDI) samples per label.
- 8 bit message counters, 4 for each label, to indicate stale, fresh, or unsampled data.
- All data bits are frozen during the time data words are sampled into the output frame
- Lightning Protection per DO-160C

DESCRIPTION

NBM-A429-8 is a fully programmable 8 Channel ARINC 429 Bus Monitor Module. This module monitors and stores data from up to eight ARINC 429 data bus signals. Selected data from each ARINC 429 bus can be inserted into the PCM stream. The ARINC 429 inputs are programmable for high or low bus speeds. The module is a "listen only" unit and does not interfere with normal operation.

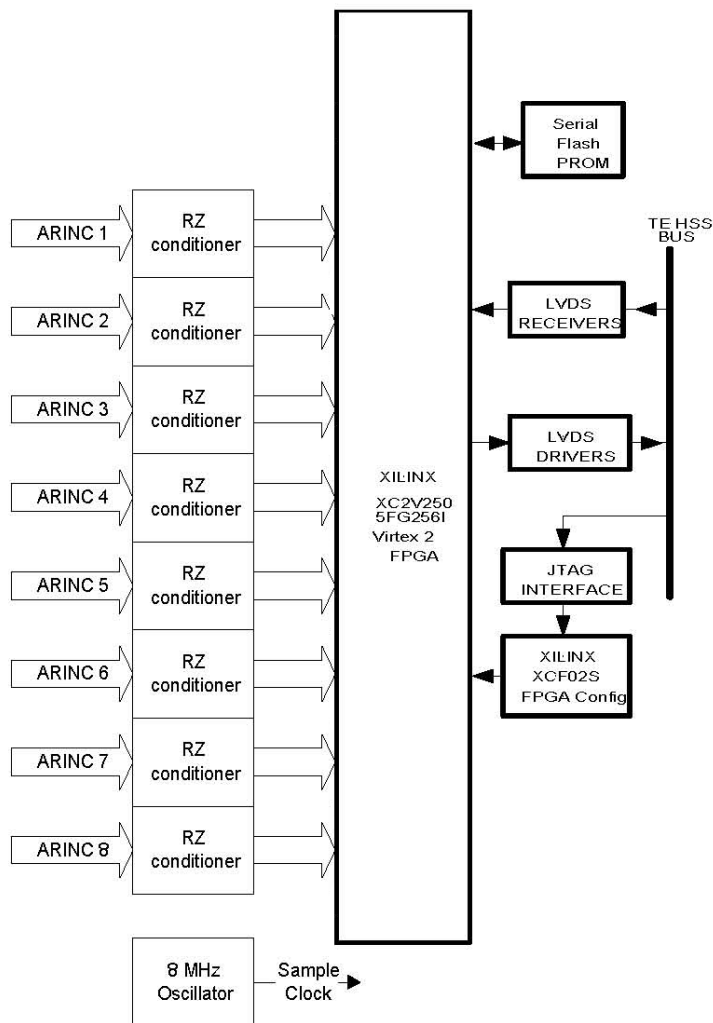
Each of the eight ARINC 429 bus signals are inputted through a MDMV37P connector mounted on top of the module.



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THEORY OF OPERATION



Each of the 8 differential ARINC-429 inputs are received into an RZ conditioner. Each conditioner provides 2 outputs to indicate a logic HI or logic LO detect on the input. If neither logic outputs are asserted, this indicates a NULL. The RZ conditioners have test inputs to allow POST testing of the detection circuitry.

A deserializer, clocked by an 8 MHz sample clock, provides word framing by counting at least 4 NULL bits. A control bit for Hi/Lo speed operation determines the count interval. Upon achieving frame lock, HI and LO bits are shifted into a 32 bit shift register after consistent sampling of a steady bit level for 3 clocks. A NULL level for at least 3 clocks indicates the end of the bit. After all 32 bit have been shifted and the word frame is detected, the deserializer performs parity checking. If parity checks are OK, the deserializer asserts a new word request. If a parity error is detected, the message is discarded and the error is latched for reporting later.

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