



FEATURES

- 2 independent bit sync channels
- Bit Rates to 20 Mbps NRZ codes, 10 Mbps BiØ codes, 40 Mbps QPSK
- Performance within 1 dB of theory
- Accepts NRZ-L/M/S, BiØ-L/M/S, DBiØ-/LM/S, DM-M/D, MDM-M/D codes
- Two single-ended and one differential input per channel
- Selectable PCM outputs at TTL, RS-422, or Bipolar levels.
- Selectable Output Clock (0°, 90°, 180°, 270°)
- PN Randomizer/Derandomizer per IRIG STD 106-96
- Viterbi Decoding with constraint length $k=7$ and rate $R=1/2$
- Convolutional De-interleaving per NASA 530 SNUG REV 7
- Resequencer for QPSK/OQPSK Mode
- Special Rate 1/3 Shuttle Viterbi Decoding available

DESCRIPTION

The Model 3362 is a full function 20 Mbps tunable Dual Channel QPSK PCM Bit Synchronizer in a 3 rack-unit chassis. It is ideally suited for reconstructing a noisy input PCM data stream and providing a clean PCM signal with a coherent clock. The unit can be operated as a single or dual channel bit synchronizer. By providing Dual Channels, I and Q outputs from a QPSK receiver demodulator may be processed and recombined into a single output.

Each channel of the Model 3362 is tunable over the bit rate range of 10 bps to 20 Mbps for NRZ codes and up to 10 Mbps for BiØ codes. The standard NRZ-L/M/S, BiØ-L/M/S, DBiØ-M/S, DM-M/S, MDM-M/S codes are accepted from one of three input sources. The 3362 produces an output data stream with a bit error rate within 1 dB of theory. The 3362 excels in BER performance, offering enhanced sync maintenance and acquisition capabilities. It maintains effective synchronization down to an E_b/N_0 of -3 dB and acquisition time is less than 20 transitions in noise. The loop bandwidth can be set anywhere in the range from 0.01% to 1.60% without losing phase lock.



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Programmable randomizer and derandomizer are included for generation of a randomized serial data output and derandomizing of the data from an external source.

Two single-ended inputs and one differential input per channel are standard. The single-ended input impedance is selectable between 75 ohms or 10k ohms. The selected noise input is gain-controlled and corrected for dc offset. It is then supplied to a matched filter. The peaks of the filtered signals are detected to reconstruct the PCM data streams. The internal clock is locked to the input signal through a phase-locked loop circuit. Differences between the selected clock rate and input signal rate develop loop correction voltages that synchronize the clock with the data.

An abundance of outputs provide for flexibility in integrating the Model 3362 into your system. A selectable PCM output and a programmable clock (0°, 90°, 180° and 270°) are available at TTL and RS-422 levels for each channel. A bipolar PCM output is also provided. For systems requiring forward error corrections, 3-bit soft decision outputs are fed to the internal Viterbi decoder.

SPECIFICATIONS

<u>FUNCTION</u>	<u>CHARACTERISTICS</u>	<u>MECHANICAL</u>	
Bit Rate	10 bps to 20 Mbps for NRZ codes, 10 Mbps for BiØ codes.	Size	19" Rack Mount, 5.25" High,
Input Source	Selectable: Two single-ended, one differential channel	Weight	Less than 35 lbs.
PCM Codes	Accepts NRZ-L/M/S, BiØ-/L/M/S, DBiØ-L/M/S, DM-M/S, Randomized, derandomizer per IRIG STD 106-96	Operating Altitude	15,000 ft
S/N Performance	Reconstructs data to within 1 dB of ideal bit error probability curves to Eb/No of 0 dB	Storage Altitude	30,000 ft
		Operating Temperature	0 to 50 degrees C
		Storage Temperature	-20 to 70 degrees C
		Humidity	To 95% non-condensing
		Power	115/230 VAC 50-400 Hz Automatic Selection

SPECIFICATIONS SUMMARY

Input	
Selection	1 of 3
Input 1 and 2	
Type	Single-ended
Impedance	75Ω (50Ω optional) or 10 KΩ.
Input 3	
Type	Differential
Impedance	75Ω
Polarity	Normal or inverted (NRZ-L and Biφ-L codes only)
Direction	Forward or Reverse (Biφ-L code only)
Amplitude	Single-ended: 100 mVpp to 10 Vpp Differential: 200 mVpp to 8 Vpp
Baseline Shift	No degradation in performance for baseline shifts up to 100% peak-to-peak signal amplitude.
Baseline Variation	No degradation in performance for a superimposed waveform whose amplitude is equal to the peak-to-peak amplitude of the PCM input signal and whose frequency is up to 0.1% of the bit rate.
PCM Codes	NRZ-L/M/S, Biφ-L/M/S, DBiφ-M/S, DM-M/S, MDM-M/S, RNRZ-L (Note 1)
Bit Rate Range	10 bps to 20 Mbps NRZ codes and maximum 10 Mbps for all other codes.

Synchronization	
Acquisition	Acquires synchronization reliably on input signals with Eb/No to 0 dB and 50% transition density.
Acquisition Range	Within ± 5% of selected bit rate and Eb/No to 15 dB.
Tracking	Tracks to bit rate variations up to ± 20% of selected bit rate after acquisition with Eb/No to 15 dB
Retention	Retains synchronization on input signals with transition gaps up to 128 bit periods once every 512 random bits for Eb/No to 3 dB.
Synchronization Maintenance	Maintains synchronization to Eb/No of 0 dB for NRZ, Biφ and DBiφ codes. (Note 2)
Loop Bandwidths	Tunable from 0.01% to 1.6% of bit rate without causing loss of synchronization.
Phase Ambiguity Resolution	Resolves phase in Biφ codes having 100 random bit periods and maintains phase up to 2000 constant logic 1 or 0 bits for Eb/No to 15 dB.
S/N Performance	Reconstructs data to within 1 dB of the ideal bit error probability curves with Eb/No to 0 dB. (Note 2)

Serial Output	
PCM 1 (Note 4)	
Data	
Code	NRZ-L/M/S, Bi ϕ -L/M/S, or RNRZ-L (Note 1)
Levels	Selectable: TTL (+3V into 50 Ω), RS422 (Differential) or Bipolar (2Vpp into 50 Ω) (Note 4)
Clock	
Phase	0 $^\circ$, 90 $^\circ$, 180 $^\circ$ or 270 $^\circ$ (Note 3)
Duty Cycle	50/50 (67/33 when Rate 1/3 selected) \pm 5%
Skew	\leq 1/8 of a bit period
Levels	TTL (+3V into 50 Ω) or RS422 (Differential)
PCM 2 (Note 4)	
Data	
Code	NRZ-L/M/S, Bi ϕ -L/M/S, or RNRZ-L (Note 1)
Levels	Selectable: TTL (+3V into 50 Ω), RS422 (Differential) or Bipolar (2Vpp into 50 Ω) (Note 4)
Clock	
Phase	0 $^\circ$, 90 $^\circ$, 180 $^\circ$ or 270 $^\circ$ (Note 3)
Duty Cycle	50/50 (67/33 when Rate 1/3 selected) \pm 5%
Skew	\leq 1/8 of a bit period
Levels	TTL (+3V into 50 Ω) or RS422 (Differential)

Convolutional Deinterleaver	
Control	Bypass or Enabled
Interleaver Input	Rate 1/2 or 1/3 symbols, starting with G1 in row 0
Deinterleaver Input	3-bit soft decision, true or inverted
Delay rows	30
Delay of rows 0 through 29	4 * i (where i = 0 through 29)
Cover Sequence Length	30-bits
Synchronization	
Cover Sequence Row 0 through 29	000001110010001010111101101001
Symbol Frame Counter	10-bit counter advances each symbol frame
Acquisition Delay	1,2,3 or 4 symbol frame counter cycles
Flywheel Count	1,2,3 or 4 symbol frame counter cycles

Viterbi Decoder	
Control	Bypass or Enabled
Input symbols	3-bit Soft decision
Constraint Length	7
Rates	1/2 or 1/3
Generator Polynomials	
Rate 1/2	G0 = 171 ₈ , G1 = 133 ₈
Rate 1/3	G0 = 171 ₈ , G1 = 133 ₈ , G2 = 165 ₈

Differential Decoders	
Type 1	BPSK (single NRZ M to L)
Control	Bypass or Enabled
Type 2	SQPSK (dual NRZ M to L)
Control	Bypass or Enabled
Type 3	QPSK (Permi Select)
Control	Bypass or Enabled
Permutation Select	1 of 24

Derandomizer	
Type	Programmable Tap Selection (1 through 24)
Control	Bypass or Enabled

Resequencer	
Control	Bypass or Enabled
Modulation	BPSK, QPSK or OQPSK
Order	AB or BA
Polarity	Bypass, Invert A or Invert B
Framer	
Control	Bypass or Enabled
Input Polarity	Normal or Automatic Polarity Correction
Sync Strategy	Normal or Quick
Frame length	16 to 1048756 bits
Bit slip window	Selectable: off, ±1, ±2, ±3
Frame sync location	First or Last word in the frame
Frame sync pattern	4 to 64 contiguous bits with mask
Pattern type	Normal, Alternate Frame Sync, or Complement Frame Sync
Search / Lock error thresholds	0 to 15 errors (independently programmed)
Check / Flywheel patterns	0 to 15 patterns (independently programmed)
Sync states	search, check, lock, flywheel

NOTES:

1. Bi ϕ -M and Bi ϕ -S comply with IRIG STD 106-96 and are the same as DBi ϕ -M and DBi ϕ -S respectively in IRIG 106-93. RNRZ-L is programmable up to 24-bits (this includes the IRIG STD 106-86). For rate 1/3 Viterbi, only the NRZ codes are available.
2. Assumptions: Gaussian noise; random, square-sided PCM with 50% transition density; narrow loop bandwidth.
3. For rate 1/3 Viterbi, only the 0° or 180° clock is available.
4. There is only 1 each of the physical outputs (TTL, RS422, and bipolar) that can be driven by PCM 1 or PCM

www.L-3Com.com/te



L-3 Communications Telemetry-East
1515 Grundy's Lane
Bristol, PA 19007
Tel: 267-545-7000
Fax: 267-545-0100



L-3 Communications Telemetry-West
9020 Balboa Avenue
San Diego, CA 92123-3507
Tel: 858-694-7500, 800-351-8483
Fax: 858-279-0693